Application No. 09/909,934
Filed: July 20, 2001
Group Art Unit: 2827

REMARKS

The specification, drawing, and claims have been amended as set forth above. Claims 1-7 as amended are pending.

In the Office Action, Figure 1 was objected to for including a reference number 24 pointing to no structure and for lacking the legend "Prior Art". It is believed that these objections are overcome by amended Figure 1. Also, Figure 2 was objected to for including characters and numbers not referred to in the specification. It is assumed that the characters and numbers that are objected to are those near the bottom of Figure 2, which are not reference numbers. These have been deleted. All the reference numbers (1, 10-12, and 14-16) are referred to in the specification.

The amendments to the Specification are to delete the use of the reference number "24" and to provide clear support for the term "integrated circuit areas" which has been introduced to address an objection under 35 U.S.C. § 112, 2nd para. (see below). No new matter has been entered.

In the Office Action, claims 1-7 are rejected under 35 U.S.C. § 112, 2nd para., for a variety of reasons, each of which is believed to be addressed by the amendments herein. Specifically, the double recitation of "lead frame" has been deleted; the term "integrated circuit" has been changed to "integrated circuit

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313

areas" to clarify that each die pad is part of an integrated circuit area of the lead frame; and "holes" and "slots" have been further described as being non-elongated and elongated, respectively. With respect to the objection to claim 5, claim 5 has been amended to refer to each of the plurality of interlocking means recited in claim 2, and therefore it is believed that sufficient antecedent basis now exists.

In the Office Action, claims 1-7 are rejected under 35 U.S.C. § 103(a) as being obvious in view of Kajihara (US 5,637,913) and Yang (6,043,109). This rejection is respectfully traversed.

Claim 1 recites a stress-free lead frame having a plurality of integrated circuits areas, each integrated circuit area having a die pad and a plurality of leads, and a peripheral pad surrounding the plurality of integrated circuit areas. The peripheral pad is provided with a plurality of stress-relief means. Examples of the stress-relief means include non-elongated holes and elongated slots, as recited in claim 3. As described in the specification, when the interior portion of the lead frame with integrated circuit areas is subject to the heat of injection molding, the stress-relief means allows for expansion and compression of the leads notwithstanding that the relatively cold periphery of the lead frame does not expand and compress to the same degree. As a result, there is less of the type of stress on

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the leads that can cause harmful delamination, so that manufacturing yields of packaged ICs are improved.

Kajihara is seen to show a lead frame with a die pad 3 and a plurality of leads 5, as correctly noted in the Office Action. The die pad 3 is suspended by suspension leads 4 that extend outwardly to a dam bar 7. In the embodiment of Figure 16, referred to in the Office Action, small pads 20 are arranged on the suspension leads 4 near the die pad 3. Each small pad 20 has a central hole. Each suspension lead 4 also has openings (unnumbered) on an outer portion between the corresponding pad 20 and the dam bar 7.

It is noted that Kajihara's small pads 20 contain only one opening. Further, the small pads 20 and suspension leads 4 are part of the mounting structure for a single integrated circuit, and in fact partly define the area in which a single integrated circuit is to be mounted. Thus, rather than surrounding a plurality of integrated circuit areas, as implicitly suggested in the Office Action, the small pads 20 and suspension leads 4 of Kajihara are themselves part of a single integrated circuit area that is surrounded by separate structure, including dam 7 and frame members 8 and 9.

Yang shows a method of fabricating circuits consisting of two attached semiconductor dies 200 and 302. At one point in the

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FAX. (617) 451-0313

fabrication process (e.g., Fig. 3B), it appears that a plurality of dies 200 are attached and wired to corresponding sites on a multi-die wafer 300, each site having one of the dies 300. The wafer 300 is then sawed along scribe lines 304 to yield multiple 2-die circuits, such as shown in Fig. 3C.

Yang is not seen to provide any teaching with respect to leadframes, nor with respect to the problem of delamination of leadframe leads from a molded epoxy package during a process of fabricating a packaged IC.

It is respectfully submitted that the combination of Kajihara and Yang cannot render the invention of claim 1 obvious. Neither of these references teaches or suggests a leadframe having a peripheral pad that includes stress-relief means and that surrounds a plurality of integrated circuit areas, where each integrated circuit area includes a die pad and leads, as set forth in claim 1. As described above, Kajihara's small pads 20 and suspension leads 4 do not surround a plurality of integrated circuit areas; they extend away from only a single die pad 3. In fact, the pads 20 and leads 4 actually constitute part of the mounting for a single die. Therefore, these components in Kajihara do not constitute a peripheral pad that surrounds a plurality of integrated circuit areas, where each integrated circuit area includes a die pad and leads.

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FAX. (617) 451-0313

Furthermore, Yang is not seen to teach such a peripheral pad either, and in fact the Office Action has not alleged any such teaching in Yang. Rather, the Office Action notes only that Yang teaches fabricating multiple chips next to one another and then dicing them apart "for the purpose of reducing package volume", and states that "it would have been obvious...to incorporate the teachings of Yang to those of Kajihara ... to reduce package volume." This statement is not seen to provide the teaching that is missing from these reference individually. As noted above, Yang's arrangement utilizes individual dies 200 mounted on a wafer 300, and does not utilize a leadframe. It is entirely unclear whether the teaching of Yang can be applied to that of Kajihara in any meaningful way. If the Office Action is suggesting only that Yang somehow motivates one of ordinary skill to utilize a leadframe to make multiple packaged ICs at a time, Kajihara already teaches this at column 5, line 66 to column 6, line 2. In this regard, note that the outer frame 8 is depicted as extending further right and left in the Figures. However, neither Kajihara nor Yang describes any need to add stress relief means to the outer frame 8 or to any other structure that connects multiple integrated circuit areas of a leadframe together. Because these references fail to teach this feature of claim 1, these references

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TEL. (617) 542-2290
FAX. (617) 451-0313

cannot render the invention of claim 1 obvious under 35 U.S.C. § 103.

Claims 3, 4 and 6 are dependent from claim 1, and therefore the above discussion likewise applies to the patentability of these claims over Kajihara and Yang.

Claim 2 is similar to claim 1 except in reciting that the peripheral pad is provided with a plurality of interlocking means, which can constitute elongated slots in one embodiment. It will be observed that the combination of Kajihara and Yang do not teach this feature of claim 2, and therefore claim 2 is not rendered obvious by these references under 35 U.S.C. §103(a).

Claims 5 and 7 are dependent from claim 2, and therefore the above discussion likewise applies to the patentability of these claims over Kajihara and Yang.

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GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451 0313

In view of the foregoing, it is believed that the rejections under 35 U.S.C. § 112 and 35 U.S.C. § 103(a) have been overcome, and that therefore this application is in condition for allowance. Favorable action is respectfully requested. The Examiner is encouraged to telephone the undersigned attorney to discuss any matter that would expedite allowance of the present application.

Respectfully submitted,

LEE KOCK HUAT ET AL.

By: James F. Thompson

James F. Thompson
Registration No. 36,699
Attorney for Applicant(s)

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP

Ten Post Office Square
Boston, MA 02109
Telephone: (617) 542-2290
Telecopier: (617) 451-0313

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288369-1

WEINGARTEN, SCHURGIN,
GAGNEBIN & LEBOVICI LLP
TEL. (617) 542-2290
FAX. (617) 451-0313